AMENDMENTS TO THE SPECIFICATION

Please amend the specification. Please replace paragraph **[0036]** in the specification with the following paragraph:

The WAN Interface Sublayer (WIS) 330, in one embodiment, is used as a SONET packet framer/deframer. Under normal operating conditions, LAN data is first encoded using an industry known 64B/66B encoding standard, and then the raw serial data is transmitted at a data rate of approximately 10.31 GHz. In contrast, the SONET infrastructure and technology powering WAN networks encodes the raw serial data into ~~packets~~ frames prior to transmission.

Please replace paragraph **[0037]** in the specification with the following paragraph:

It will be appreciated that even in WAN mode, data still will come from PCS and 64B/66B encoder 320. To be able to communicate with a WAN network, an embodiment of the present invention provides a WIS 330 configured to extract Ethernet data from the payload areas of incoming SONET packets. The WIS 330 may also be configured to encode Ethernet data received from the Physical Coding Sublayer (PCS) 320 into the payload areas of blank SONET-~~packets~~ frames prior to transmission. In passing, note that a LAN embodiment of communications system 300 may omit WIS 330.

Please replace paragraph **[0039]** in the specification with the following paragraph:

Media Access Control (MAC) sublayer 310, receives the decoded Ethernet frames and passes the data 381 to the appropriate destination address in Application Layer 312. MAC layer 310 also receives data 391 from Application Layer 311, and packages it into Ethernet frames together with a Destination Address, Source Address, and other information required by IEEE Standard 802.3. Once packaged, the Ethernet-~~Frames~~ packets are sent over XGMII or XAUI 313 to PCS 320 for coding. If communications system 300 is linked to a LAN network, the coded Ethernet data bypasses WIS 330 and funnels directly into serializer 350, which serializes the data and bumps up the data rate to approximately 10.31 GHz for transmission via PMD 370. On the other hand, if communications system 300 is linked to a WAN network, the coded Ethernet data is forwarded to WIS 330, where it is loaded into the payload areas of SONET-~~packets~~ frames. The loaded SONET-~~packets~~ frames are then forwarded in parallel over XSBI 314 to serializer 350, which serializes the data stream and bumps up the data rate to approximately 9.95 Ghz for transmission via PMD 370. It will be appreciated that in the SONET world the XSBI 314 interface is called SF14 and is defined by the Optical Internetworking Forum.

Please replace paragraph **[0042]** in the specification with the following paragraph:

Referring again to **Figure 4**, an embodiment of deserializer 405 includes a frequency and phase lock unit 430, a data rate detection unit 420, a frequency selector unit 435, and a frequency configuration unit ~~440~~ 425. Data line 415 represents the incoming data stream received from a remote LAN or WAN network (not shown). Data line 415 take the form of conventional data transfer mediums, such as a data bus. Data rate detection unit 420 samples the phase rate of the incoming data stream and determines the rate of data transfer, e.g. 10.31 GHz or 9.95 GHz. The determined data rate is then conveyed to the frequency configuration unit ~~440~~ 425, which coordinates the process of locking to the incoming data stream by managing frequency selector unit 435 and

frequency and phase lock unit 430. In one embodiment, dual external reference oscillators (clocks) 480 and 490 are provided to generate a plurality of reference frequencies that may be used to phase lock the incoming data stream. In one embodiment oscillator 480 generates WAN frequencies and oscillator 490 generates LAN frequencies.

Please replace paragraph **[0050]** in the specification with the following paragraph:

Referring again to Figure 5, the serializer 504 of SERDES device 500 is configured to automatically switch between LAN and WAN modes in response from control commands received from the deserializer 505, because DRSO 507 and DRSI 508 are connected. However, in another embodiment shown in Figure 6, the auto-configuration of serializer ~~604~~ 620A may be disabled by decoupling DRSO ~~607~~ 650A and DRSI ~~608~~ 660A as shown.

Please replace paragraph **[0051]** in the specification with the following paragraph:

Referring back to Figure 5, an illustrative auto-configuration process is now described. At startup, the Voltage Controlled Oscillator ~~(VC0)~~ (VCO) **525** frequency of the deserializer 505 is aligned to one of the two available external reference clocks, X02 and X01, and the device will attempt to phase lock to the incoming data. If the serial data is at a different, relative frequency, the deserializer 505 will switch to the other reference clock, align the VCO **525** to this frequency, and attempt to phase lock to the input data.